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	Application No.	Applicant(s)	
Notice of Allowability	09/741,999	MODELSKI ET AL.	
	Examiner	Art Unit	:
	Tony Mahmoudi	2165	
The MAILING DATE of this communication appear All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in ) or other appropriate common IGHTS. This application is s	n this application. If not included unication will be mailed in due course. <b>TH</b>	IS iative
1. This communication is responsive to the amendment filed	on 30-August-2005.		
2. The allowed claim(s) is/are 2-4, 6-16 and 18, re-numbered	l as claims 1-15.		: •
3. ☐ Acknowledgment is made of a claim for foreign priority up a) ☐ All b) ☐ Some* c) ☐ None of the:  1. ☐ Certified copies of the priority documents have 2. ☐ Certified copies of the priority documents have 3. ☐ Copies of the certified copies of the priority documents have a lateractional Purson (POT Pule 17.2(c))	e been received. e been received in Applicatio	on No	ne
International Bureau (PCT Rule 17.2(a)).  * Certified copies not received:			:
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.  4. A SUBSTITUTE OATH OR DECLARATION must be subm	MENT of this application.		
INFORMAL PATENT APPLICATION (PTO-152) which giv			• •
5. CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.			:
(a) including changes required by the Notice of Draftspers		w ( PTO-948) attached	:
1) hereto or 2) to Paper No./Mail Date	=	in the Office setting of	
(b) ☐ including changes required by the attached Examiner' Paper No./Mail Date	s Amendment / Comment of	rin the Office action of	
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t			
6. DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT			: : •
		·	
Attachment(s)  1. Notice of References Cited (PTO-892)	5 Niction of In	oformal Patent Application (PTO-152)	
<ol> <li>Notice of References Cited (PTO-692)</li> <li>Notice of Draftperson's Patent Drawing Review (PTO-948)</li> </ol>	6. ⊠ Interview S	ummary (PTO-413),	
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0		/Mail Date <u>20050916</u> . Amendment/Comment	:
Paper No./Mail Date  4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	8. ⊠ Examiner's 9. ☐ Other	Statement of Reasons for Allowance  Control of Reasons for Allowance  Control of Reasons for Allowance	

### **DETAILED ACTION**

### Remarks

- 1. In response to the amendment filed on 30-August-2005, claims 1 and 5 are canceled and claims 2-4 and 6 are amended per applicant's request. Therefore, claims 2-4, 6-16 and 18 are pending in the application, of which, claims 2 and 6 are presented in independent form.
- 2. In view of the examiner's amendment, authorized by the Attorney of Record, claims 2, 5 and 6 are further amended by the examiner (details provided below.)

## Examiner's Amendment

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. David A. Dagg (Attorney of Record) on 16-September-2005 (see enclosed Interview Summary, paper No. 20050916.)

Claims 2, 5 and 6 are amended by the examiner as follows:

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2. (Currently Amended) A method for direct access to bit fields in instruction operands, further comprising:

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providing indications of bit fields in source and target operands of a processor executable instruction, each of the indicated bit fields consisting of a plurality of bits in a plurality of bit positions in the source and target operands;

performing the processor executable instruction utilizing the bit fields in the source and target operands in response to the indications of the bit fields-; and

providing, by performing the processor executable instruction, and in response to the indications of the bit fields, direct manipulation of any bits in any bit field of the source and target operands;

transferring data from an input buffer to a packet task manager;

dispatching the data from the packet task manager to an analysis machine,

classifying the data in the analysis machine; and

modifying and forwarding the data in a packet manipulator,

wherein no instruction depends on a preceding instruction because each instruction in a pipeline is executed for a different thread.

5. (Canceled) (previously presented) An apparatus for directly accessing bit fields in instruction operands, said apparatus comprising:

at least one memory;

at least one processor;

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a bus interconnecting said at least one memory and said at least one processor;

wherein one of said at least one processor retrieves indications of bit fields, said bit fields
each consisting of a plurality of bits in a plurality of bit positions within the source and target
operands for a processor executable instruction, performs the processor executable

indications of the bit fields, and provides, by performance of the processor executable

instruction utilizing the bit fields in said source and target operands in response to the

instructions, and in response to the indications of the bit fields, direct manipulation of any

bits in any bit field of the source and target operands.

6. (Currently Amended) An apparatus for directly accessing bit fields in instruction operands, comprising:

at least one memory;

at least one processor;

a bus interconnecting said at least one memory and said at least one processor;

wherein one of said at least one processor retrieves indications of bit fields, said bit fields each consisting of a plurality of bits in a plurality of bit positions within the source and target operands for a processor executable instruction, performs the processor executable instruction utilizing the bit fields in said source and target operands in response to the indications of the bit fields, and provides, by performance of the processor executable instructions, and in response to the indications of the bit fields, direct manipulation of any bits in any bit field of the source and target operands; and

wherein the processor comprises:

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an analysis machine having multiple pipelines,

a packet task manager operationally connected to said analysis machine, and a packet manipulator operationally connected to said analysis machine.

### Allowance

- 4. Claims 2-4, 6-16 and 18 are allowed over the prior art made of record.
- 5. The following is an examiner's statement of reasons for allowance:

The applicant's amendment, filed on 30-August-2005, overcomes the cited prior art with respect to the newly amended independent claims 2 and 6. Both independent claims have been amended by the applicant to include allowable subject matter(s), as indicated by the examiner in the previous Office Action, dated 04-May-2005.

The examiner's amendment, authorized by the attorney of record on 16-September-2005, overcome the duplicate claim conflict (claim 5) and overcomes minor informalities (claim 2), and 35 U.S.C 112, second paragraph issues, lack of antecedent basis (claim 6.)

The prior art of record, Narad et al (U.S. Patent No. 6,157,955), Hansen et al (U.S. Publication No. 2004/0049663 A1), Christie et al (U.S. Patent No. 6,157,996), Islam et al (U.S. Publication No. 2003/0035430 A1), Stuttard et al (U.S. Publication No. 2002/0174318 A1), do not disclose, teach, or suggest the claimed limitations of (in combination with all other features in the claim):

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transferring data from an input buffer to a packet task manager;
dispatching the data from the packet task manager to an analysis machine;
classifying the data in the analysis machine; and

modifying and forwarding the data in a packet manipulator,

wherein no instruction depends on a preceding instruction because each instruction in a pipeline is executed for a different thread, as recited in independent claim 2.

Claims 3 and 4 are allowed over the prior art made of record because they depend from the allowed independent claim 2.

The prior art of record, Narad et al (U.S. Patent No. 6,157,955), Hansen et al (U.S. Publication No. 2004/0049663 A1), Christie et al (U.S. Patent No. 6,157,996), Islam et al (U.S. Publication No. 2003/0035430 A1), Stuttard et al (U.S. Publication No. 2002/0174318 A1), do not disclose, teach, or suggest the claimed limitations of (in combination with all other features in the claim):

an analysis machine having multiple pipelines;

a packet task manager operationally connected to the analysis machine; and,

a packet manipulator operationally connected to the analysis machine, as recited in independent claim 6.

Claims 7-16 and 18 are allowed over the prior art made of record because they depend from the allowed independent claim 6.

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# Conclusion

6. Any inquiries concerning this communication or earlier communications from the examiner should be directed to Tony Mahmoudi whose telephone number is (571) 272-4078. The examiner can normally be reached on Mondays-Fridays from 08:00 am to 04:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffery Gaffin, can be reached at (571) 272-4146.

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September 19, 2005